96. The semiconductor wafer of Claim 95, wherein said one or more layers of upper metal lines are separated by organic dielectric layers.

97. The semiconductor wafer of Claim 95, wherein upper contact pads are formed in a top layer of said one or more layers of said upper metal lines.

98. The semiconductor wafer of Claim 97 wherein solder bumps are formed on said upper contact pads.

99. The semiconductor wafer of Claim 95, wherein said upper metallization structure is configured to provide fan-out, relocation and reduction capabilities.

REMARKS

Please enter this Preliminary Amendment in the above referenced Divisional patent application. All claims are believed to be allowable.

Changes are shown in the attached "Version to Show Marked-up Changes"

Should there be any question regarding this Amendment, please contact the undersigned attorney at (845)-452-5863.

Respectfully Submitted,

Stephen B. Ackerman

Reg. No. 37,761

Version to Show Marked-up Changes

PLEASE AMEND THE SPECIFICATION AS FOLLOWS:

Please replace the 1st paragraph under "Summary of the invention" with the following paragraph:

It is the primary objective of the present invention [is] to improve the performance of High Performance Integrated Circuits.

Please replace the last paragraph on page 12 with the following paragraph:

The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD) oxide and nitride. In creating layer 4, a layer of approximately 0.2 um. PECVD oxide is deposited first followed by a layer of approximately 0.7 um. nitride. Passivation layer 4 is very important because it protects the device wafer from moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron process (of the interconnecting metallization structure) is of critical importance since it allows for a cheaper process that possibly has less

stringent clean room requirements for the process of creating the interconnecting metallization structure.

Please replace the last paragraph on page 17 with the following paragraph:

Fig. 6 shows a basic design advantage of the invention. This advantage allows for the sub-micron or fine-lines, that run in the immediate vicinity of the metal layers 3 and the contact points 6, to be extended in an upward direction 20 through metal interconnect 7'[,]. T[t]his extension continues in the direction 22 in the horizontal plane of the metal interconnect 26 and comes back down in the downward direction 24 through metal interconnect 7". The functions and constructs of the passivation layer 4 and the insulating layer 5 remain as previously highlighted under Fig. 1. This basic design advantage of the invention is to "elevate" or "fan-out" the fine-line interconnects and to remove these interconnects from the micron and sub-micron level to a metal interconnect level that has considerably larger dimensions and is therefore [with] chacterized by smaller resistance and capacitance and is easier and more cost effective[ly] to manufacture. This aspect of the invention does not include any aspect of conducting line re-distribution and therefore has an inherent quality of simplicity. It therefore further adds to the importance of the invention in that it makes micron and sub-micron wiring accessible at a wide-metal level. The interconnections 7' and 7" interconnect the fine-level metal by going up through the passivation and

polymer or polyimide dielectric layers, tra[ns]verses over a distance on the wide-metal level and continues by descending from the wide-metal level back down to the fine-metal level by again tra[ns]versing down through the passivation and polymer or polyimide dielectric layers. The extensions that are in this manner accomplished need not to be limited to extending fine-metal interconnect points 6 of any particular type, such as signal or power or ground, with wide metal line 26. The laws of physics and electronics will impose limitations, if any, as to what type of interconnect can be established in this manner where limiting factors will be the conventional limiting factors of resistance, propagation delay, RC constants and others. Where the invention is of importance is that the invention provides much broader latitude in being able to apply these laws and, in so doing, provides a considerably extended scope of the application and use of Integrated Circuits and the adaptation of these circuits to a wide-metal environment.

Please replace page 22, second paragraph, with the following paragraph:

Fig. 10 shows the concept of pad relocation. BGA pad 120 [can be] connects to any of the contact balls 101 through 105. By using the BGA substrate 130 and the wiring 131 that is provided within the substrate, it is clear that the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging. For instance contact point 101, which is on the far left side of the BGA device 100, is re-routed to location [121]

122 which is on the second far right of the BGA substrate 130. The re-arrangements of the other BGA solder bumps can readily be learned from following the wiring [130] 131 within the substrate 130 and by tracing from solder bump to one of the contact points 122 through 125 of the BGA substrate.

page 22, after the second paragraph, please add the following new paragraphs:

The concept of pad relocation can be realized using the metal interconnection scheme described in this invention, to replace the function of BGA substrate 130. From Figs. 10 and 11 it can be seen that the extended functionality and extended wiring ability that are provided by the interconnect wiring schemes that are typically created in the BGA substrate 130 can be created using the method of the invention, on device 100. Some of the methods and possibilities of interconnect line routing that can be implemented using the method of the invention are highlighted in the following paragraphs.

Fan-out capability can be provided by the invention, using the metal conductors within the openings through the insulating layer and through the passivation layer that connect electrical contact pads of the top metallization structure with contact points of the interconnecting metallization structure. Each of the electrical contact points of the interconnecting metallization structure is

connected directly and sequentially with at least one electrical contact point of the top metallization structure. In a fan-out scheme, the distance between electrical contact points of the top metallization structure is larger than the distance between electrical contact points of the interconnecting metallization structure by a measurable amount.

The number of electrical contact pads of the upper metallization structure can exceed the number of contact points of the interconnecting metallization structure by a considerable amount.

Pad relocation may also be accomplished by the method of the invention. Electrical contact points of the top metallization structure are connected with the contact points of the interconnecting metallization structure, directly but not necessarily sequentially, thereby creating a pad relocation effect. In this method, the distance between electrical contact points of the top metallization structure is larger than the distance between the electrical contact point of the interconnecting metallization structure by a measurable amount.

A reduction effect may also be accomplished by the method of the invention, wherein common nodes are connected together. Electrical contact points on a top surface of the top metallization structure are connected with contact points of the interconnecting metallization structure, where fewer contact points are used in the top metallization structure, since functionally equivalent